UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

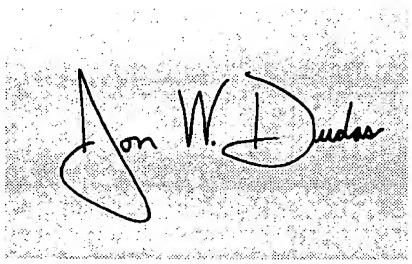
PATENT NO. : 7,007,130 B1
APPLICATION NO. : 09/023170
DATED : February 28, 2006
INVENTOR(S) : Holman et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

DELETE COLUMNS 21 LINES 18 THROUGH COLUMNS 24 LINES 4 AND INSERT THE ATTACH CLAIMS

Signed and Sealed this

Tenth Day of April, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office

Amendments to the Claims:

Please amend the claims as follows:

1. (Currently Amended) A method, comprising:

receiving, at a memory module controller of a memory module having a plurality of memory devices, a memory request signal from a system memory controller over a system memory interconnect bus; and

in response to the memory request signal, causing the memory module controller to generate a separate signal addressed to and to be serviced by at least one of the plurality of memory devices in a manner ~~regardless~~ independent of any difference of signal impedance or operating voltage between the memory devices and the system memory interconnect bus.

2. (Currently Amended) The method of claim 1, further comprising generating a separate clock signal via a clock generator within the memory module controller to drive the separate signal, the separate clock signal being different than a clock signal of the system memory interconnect bus.

3. (Original) The method of claim 1, further comprising:

examining the memory request signal to determine whether the memory request signal is addressed to at least one of the memory devices of the respective memory module; and

bypassing the memory request signal if the memory request signal is not addressed to any of the memory devices of the memory module.

4. (Original) The method of claim 3, further comprising reducing at least a portion of a power associated with the plurality of memory devices if the memory request signal is not addressed to any of the memory devices.

5. (Original) The method of claim 3, further comprising reducing a frequency of the separate clock signal with respect to the plurality of memory devices if the memory request signal is not addressed to any of the memory devices.

6. (Currently Amended) The method of claim 3, further comprising decoupling the plurality of memory devices from the system memory interconnect ~~bus~~ if the memory request signal is not addressed to any of the memory devices, such that the plurality of memory devices remain inactive.

7. (Original) The method of claim 3, further comprising providing the separate clock signal and power to the memory devices of the memory module only if the memory request signal is addressed to at least one of the memory devices.

8. (Original) The method of claim 1, wherein the plurality of memory devices and the system memory controller operate at different power voltages.

9. (Original) The method of claim 1, wherein the plurality of memory devices and the memory controller operate at different operating frequency signals having different voltage swings.

10. (Currently Amended) A system, comprising:

a memory interconnect ~~bus~~;

a system memory controller coupled to the memory interconnect ~~bus~~; and

a first memory module coupled to the memory interconnect bus, the first memory module including

a first plurality of memory devices

and

a first memory module controller coupled to the first plurality of memory devices and the memory interconnect bus to receive a memory request signal from the system memory controller via the memory interconnect bus,

in response to the memory request signal, the first memory module controller, to generate a separate signal addressed to and to be serviced by at least one of the plurality of memory devices in a manner regardless independent of any difference of signal impedance or operating voltage between the memory devices and the system memory interconnect bus.

11. (Currently Amended) The system of claim 10, wherein the first memory module controller further comprises a clock generator to generate a clock signal to drive the separate signal, wherein the clock signal is different than a clock signal of the memory interconnect bus.

12. (Original) The system of claim 11, wherein first memory module controller further comprises a request handling logic to examine the memory request to determine whether the memory request is addressed to at least one of the memory devices and to ignore the memory request if the memory request is not addressed to any of the memory devices.

13. (Original) The system of claim 12, wherein the first memory module controller further comprises a power management unit to control a power supplied to the memory devices.

14. (Currently Amended) The system of claim 13, wherein the first plurality of memory devices and the memory interconnect bus operate at different power voltages.

15. (Original) The system of claim 13, wherein the power management unit reduces at least a portion of the power to the memory devices, if the memory request is not addressed to any of the memory devices.

16. (Currently Amended) The system of claim 13, wherein the first memory module controller further comprises a control logic coupled to the request handling logic, the clock generator, and the power management unit, the control logic configured to decouple the memory devices from the memory interconnect bus if the memory request is not addressed to any of the memory devices.

17. (Original) The system of claim 16, wherein in response to a signal from the request handling logic indicating that the memory request is not addressed to any of the memory devices, the control logic instructs the clock generator to alter a frequency of the clock signal to the memory devices.

18. (Original) The system of claim 17, wherein the control logic further instructs the power management unit to disable the clock generator if the memory request is not addressed to any of the memory devices, which in turn reduces the power dissipation of the memory devices.

19. (Currently Amended) The system of claim 10, further comprising a second memory module coupled to the memory interconnect bus, the second memory module including:

a second plurality of memory devices and

a second memory module controller coupled to the second plurality of memory devices and the memory interconnect ~~bus~~, the second memory module controller managing the second plurality of memory devices independent of the first memory module controller of the first memory module and the second memory module controller separating the second plurality of memory devices of the second memory module from the system memory controller and the memory interconnect ~~bus~~.

20. (Currently Amended) The system of claim ~~19~~, wherein the first plurality of memory devices and the second plurality of memory devices have different signaling protocols, which are controlled by the first and second memory module controllers respectively, and wherein the different signaling protocols of the first and second pluralities of memory devices are incompatible with signaling protocols required by the system memory controller and the memory interconnect ~~bus~~.